

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Kiyoshi Kato                          Art Unit : Unknown  
Serial No. : New Application                      Examiner : Unknown  
Filed : April 27, 2006  
Title : SEMICONDUCTOR INTEGRATED CIRCUIT AND DESIGN METHOD  
THEREOF

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

STATEMENT REGARDING POWER OF ATTORNEY

Under 37 C.F.R. § 1.32(c)(3), please recognize the following registered patent practitioners associated with Customer No. 26171 as representatives for the above-referenced application.

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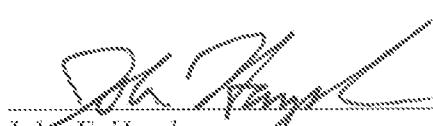
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A signed Power of Attorney for the above-identified application is attached.

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Respectfully submitted,

Date: April 27, 2006

  
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